REMARKS

Claims 1-4 and 6-26 were pending. Claims 12-13, and 21 have been cancelled. Claims 1, 9 and 18 have been amended. Accordingly, claims 1-4, 6-11, 14-20, and 22-26 remain pending subsequent entry of the present amendment.

In the present Office Action, claims 1-4 and 6-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,964,881 (hereinafter "Thor") which is also assigned to the present Applicant, in view of U.S. Patent No. 4,471,310 (hereinafter "Yenisey"). Applicant has reviewed the newly cited art and new rejections and traverses the above rejections with respect to at least some of the claims. Accordingly, Applicant requests reconsideration in view of the following discussion.

Not All Claims Addressed

Applicant notes that not all claims have been addressed in the present Office Action. For example, neither claim 13 nor its features are anywhere addressed in the present Office Action. Applicant submits the features of prior claim 13 are nowhere disclosed or suggested by the cited art, either singly or in combination. Accordingly, Applicant requests withdrawal of the rejection in view of the following discussion.

Applicant has amended claim 9 to incorporate the features of prior claim 13, and intervening claim 12. In addition, each of independent claims 1 and 18 have been amended to include the features of prior claim 13 as well. As amended, claim 9 now recites a clock circuit which includes:

> "a first circuit configured to generate a first clock signal;
> a counter configured to count sequences of pulses of said first clock signal, wherein said sequences include a fixed number of pulses; and
> circuitry configured to utilize said first clock signal to generate a second clock signal;
> wherein said second clock signal is generated with a plurality of clock frequencies, said plurality of clock frequencies including a beginning

clock frequency, one or more intermediate clock frequencies, and an ending clock frequency;

wherein a transition from said beginning clock frequency, through said intermediate clock frequencies, to said ending clock frequency is performed in a linear manner by dropping selected pulses of said first clock signal; and

wherein said circuitry is configured to detect said selected pulses of said first clock signal, wherein said selected pulses correspond to particular counts of said pulses within said fixed number of pulses. (emphasis added).

In the above, the underlined portions of the claims generally correspond to the features of prior claim 13. Applicant submits these features are nowhere found or suggested in the cited art.

In contrast to the above, Thor discloses a system which uses a combination of a first register (STR 260) for storing a value which indicates a length of time over which the processor is to ramp up to full power, and a second register (DRR 262) which stores a value identifying a desired length of time between pulses. This value in the DRR is loaded into the clock count shift register (CCSR 282) and decreased by either right shift (i.e., divide by 2) or "countdown" each time the time shift counter (TSC 280) reaches zero. As the time between pulses decreases, the output frequency increases. Such an approach is clearly distinguished from the above cited features and the above features are nowhere suggested by Thor.

Further, Yenisey discloses a pulse generator configured to generate a plurality of signals at different frequency. Pulses may then be further grouped into sets. An eight bit control word is then applied to select from the sets to generate a signal with varying frequencies. In particular, the control/digital word then selects binary weighted sets to produce the desired number of output pulses in a specified period. Here again, the approach disclosed by Yenisey is completely different than that of claim 9, and the combination of Thor with Yenisey does not suggest the features of claim 9.

In view of the above, Applicant submits prior, unaddressed, claim 13 was allowable, and claim 9 which now includes the features of prior claim 13 is patentably distinguished from the cited art. As each of independent claim 1 and 18 include similar features, each of these claims are patentably distinguished from the cited art as well.

Applicant believes the application to be in condition for allowance. However, should the examiner believe otherwise, a telephone interview with the below signed representative at (512) 853-8866 is requested to facilitate a speedy resolution.

CONCLUSION

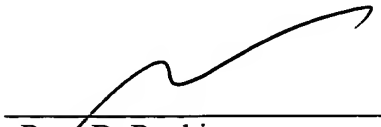
Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-80100/RDR.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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